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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/884,517 | 06/19/2001 | Eugene A. Fitzgerald | Amber.5994A | 2548 |

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| EXAMINER |
|---|
| SOWARD, IDA M |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.



paper #9

| Office Action Summary | Application No. 09/884,517 | Applicant(s) FITZGERALD ET AL. | |
|---|---|---|---|
| | Examiner KEN PIERRE | Art Unit 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) *1to 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1 to 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. This is in response to the applicant's Supplemental Information Disclosure Statement amendments received on February 08, 2002 in which applicant corrected previously submitted reference. Applicant's references including the corrected one have been fully considered and found to have no effect on the examiner previous decision. Therefore, the rejection mailed on May 7, 2002 remains.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 27 to are rejected under 35 U.S.C. 103(a) as being unpatentable over Ismail et al (5,534,713) in view of Armstrong (TECHNOLOGY FOR SiGe HETEROSTRUCTURE-BASED CMOM DEVICE) (Ph.D. THESIS SEPTEMBER 1999 AT MASSACHUSETTS INSTITUTE OF TECHNOLOGY)

Regarding claims 1, 4, 15, 18, 27, Ismail et al disclose (Col. 5, line 39 to 44) (FIG. 2) a SiGe device, comprising a relaxed SiGe buffer layer 34 that is first grown on upper surface 21 of substrate 20. (Col. 4, line 38 to 41) Field effect transistors 10 and 11 are formed on a semiconductor substrate 20 which may be, for example, silicon. (Col. 6, line 25 to 30) Silicon or $Si_{1-z}$ $Ge_z$ layer 32 is under tensile strain while layers 38

and 40 of SiGe are relaxed. (Col. 8, line 58 to 65) (FIG.5) A schematic circuit of CMOS inverter 9 is shown. Gate electrodes 16 and 17 are coupled together by way of lead 77 to provide an input to inverter 9. Drain regions 12 and 13 of field effect transistors 10 and 11. (Col.6, line 49 to 50) Over silicon layer 44, silicon dioxide layer 24 is formed.

Regarding claims 2 and 16, (Col. 9, line 37 to 40) a thin silicon layer or planarized surface such as layer 44 may be interposed between layer 32 and layer 24 to provide a better interface with layer 24.

Regarding claims 3 and 17, It is inherently known in semiconductor that the more rough is an interface layer at a device channel the higher is the surface sates or fast states and the less reliable is the device. Therefore, it is always best to keep this interface less rough as possible.

Regarding claims 5, 6, 7, 19, 20 and 21, (Col.6, line 33 to 36) in an alternate embodiment, layer 30 may have the germanium content graded within the layer. (Col.6, line 33 to 36) The electron transport to be preferred in a tensile strained Si or $Si_{1-z}Ge_z$ layer 32. (Col.2, line 50 to 55) The Ge fraction x for each layer may have its own value in the range from 0.20 to 0.5.

Regarding claims 8 to 11, the technology and geometry contribution are inherent to any transistor. For example, the ratio of the widths of n-device to the p-device is related to the molility of the electrons of the device. For a symmetric device, the ratio of

the widths of n-device to the p-device is equal to the ratio of the mobility of the electrons of the n and p devices respectively, but for a faster device, the ratio of the widths of n-device to the p-device is related to the square root of the ratio of the mobility of the electrons of the n and p devices respectively.

Regarding claims 12 to 14, (Col. 8, line 40 to 45) planar heterostructure 22 can be used in ULSI logic chips operated at high frequencies and low power consumption. (Col. 2, line 20 to 25) field effect transistor having high carrier mobility and suited for High-speed operation.

Regarding claims 22 to 25, (Col. 8, line 54 to 60) As in a CMOS circuit, other logic gates can be made such as a NAND, NOR, FLIP FLOPS, et cetera.

Regarding claim 26, it is inherent to semiconductor device physics that an inverter that uses a p-device is considered a pull-up or load transistor, and an inverter that uses an n-device is considered pull-down or driver transistor.

However, Ismail et al not disclose how to build the SiGe device with less layers of SiGe and SiGe graded.

Armstrong, discloses how to build pMOSFET and nMOSFET devices with only a few layers SiGe and SiGe graded. (Cited Thesis page 35) Strained-Si has attracted attention following the introduction of the graded buffer. (Cited Thesis page 43) Strained-Si grown on relaxed graded SiGe is very interesting because it exhibit enhance

electron while retaining high-quality silicon as silicon oxide interface. (Cited Thesis pages 49, to 53) There are different structure schemes for pMOSFET. Scheme showed in Fig. 3.2 (d) takes advantage of high hole mobility in combination of surface channel transport. (Cited Thesis pages 53 to 54) There are different structure schemes for nMOSFET Scheme showed in Fig. 3.3 (c) eliminates the need for a this Si cap layer which is difficult to maintain during processing. (Cited Thesis pages 43) In order to reduce difficulties associated with the relaxed SiGe buffer, strained SiGe on relaxed SiGe buffer have been explored.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the invention of, Ismail et al by replacing the multylayer SiGe device a relaxed SiGe layer on the Si substrate, a strained Si or SiGe on the relaxed SiGe and a buffer layer between the relaxed layer an the substrate, because, relaxed SiGe layer on the Si substrate takes advantage of high hole mobility in combination of surface channel transport and eliminates the need for a this Si cap layer which is difficult to maintain during processing, and buffer reduces difficulties associated with the relaxed SiGe buffer, strained SiGe on relaxed SiGe as taught per Armstrong reference.

***Conclusion***

3. **THIS ACTION IS MADE NON-FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this non-final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this non-final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this non-final action.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Ken Pierre whose telephone number is (703) 305-4002. The examiner can normally be reach on Monday-Friday from 8:30AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Carl Whitehead, Jr. can be reach at (703) 308-4940. The fax telephone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

4. Any inquiry of a general nature or relating to the status of this application or processing should be directed to the receptionist whose telephone number is (703) 308-0956.

KP

August 5, 2002

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800